9-13-00

A

LAW OFFICES OF
ZAGORIN, O'BRIEN & GRAHAM, L.L.P.
401 WEST 15TH STREET, SUITE 870
AUSTIN, TEXAS 78701

INTELLECTUAL PROPERTY ATTORNEYS (512) 347-9030 (PHONE) (512) 347-9031 (FAX) INTERNET: www.IP-Counsel.com

September 12, 2000

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Attorney Docket No.: 1001-0135

Transmitted herewith for filing is a patent application as follows:

Inventor(s): Charles W. Mitchell, Patrick Maupin, and Dervinn Caldwell
Title: METHOD AND APPARATUS FOR USING AN ON-BOARD TEMPERATURE SENSOR ON AN INTEGRATED CIRCUIT

Enclosed are:

- 14 Pages of Specification (including Written Description, Claims and Abstract)
- 2 Sheets of Drawings, ☒ Formal / ☐ Informal
- ☒ Declaration for Patent Application (6 pages), ☒ Executed / ☐ Unexecuted
- ☒ Assignment of the Invention (10 pages, including Cover Sheet)
- ☐ Information Disclosure Statement (_____ pages)
  - ☐ with Form(s) PTO 1449 (_____ page(s)) and copies of _____ reference(s)
- ☐ Applicant is a Small Entity. Statement filed: Herewith (_____ pages)
- ☐ Other:
- ☒ This Transmittal Letter (in duplicate) ☒ Return Postcard

CLAIMS AS FILED

	Number Filed	Number Extra	Rate	Fee
Basic Fee =				690.00
Total Claims	29 - 20	= 9	x $18.00 =	162.00
Independent Claims	4 - 3	= 1	x $78.00 =	78.00
Multiple Dependent Claims (if any) - $260.00 fee				0.00
Other:				0.00
TOTAL FILING FEE				$ 930.00

- ☐ A check is enclosed for the Total Filing Fee shown above.
- ☒ Please charge the Total Filing Fee shown above to Deposit Account 01-0365.
- ☒ The Commissioner is hereby authorized to charge any additional fees under 37 C.F.R. § 1.16 or 1.17 that may be required during the pendency of this application, and to similarly credit any overpayment, to Deposit Account 01-0365.

EXPRESS MAIL LABEL NO.:
EL675710787US

Respectfully submitted,

Mark Zagorin

Mark Zagorin, Reg. No. 36,067
Attorney for Applicant(s)
(512) 347-9030
(512) 347-9031 (fax)

"Express Mail" mailing label number:
EL675710787US

METHOD AND APPARATUS FOR USING AN ON-BOARD TEMPERATURE SENSOR ON AN INTEGRATED CIRCUIT

Charles W. Mitchell
Patrick Maupin
Dervinn Caldwell

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to integrated circuits and systems and more particularly to use of a temperature sensor on an integrated circuit.

Description of the Related Art

Computer systems have typically relied on external temperature sensors located in the proximity of the processor package to provide temperature information for thermal control. The external temperature sensor provides the temperature information to logic external to the processor, which utilizes the sensed temperature to provide appropriate thermal control functions, e.g., turning a fan on and off.

It would be desirable to incorporate temperature sensing directly onto the integrated circuit whose temperature is being measured to provide a more accurate temperature measurement of the integrated circuit die. Further, it would be desirable to provide appropriate logic on the same integrated circuit whose temperature is being measured to evaluate that temperature measurement and provide appropriate signals capable of being utilized to provide thermal control functions directly or indirectly.

SUMMARY OF THE INVENTION

Accordingly, in one embodiment, the invention provides an integrated circuit that includes a temperature sensor providing a temperature of the integrated circuit. A storage location on the integrated circuit stores a first temperature limit value. Compare logic is coupled to provide an indication of a comparison between the

temperature and the first temperature limit value. In one embodiment, the integrated circuit asserts a temperature control signal on a first output terminal when the temperature indicated by the temperature sensor is above the first temperature limit value.

In an embodiment, there are two modes of operation which can be specified to deassert the temperature control signal. In one mode, the integrated circuit deasserts the temperature control signal supplied on the first output terminal when the temperature indicated by the temperature sensor falls below a programmable second temperature limit value. In another mode, integrated circuit deasserts the temperature control signal supplied on the first output when a control location in the integrated circuit is accessed. The integrated circuit may further include an addressable storage location coupled to the temperature sensor, which supplies an indication of the temperature on the integrated circuit.

The integrated circuit may further include a second output terminal coupled to provide external to the integrated circuit an asserted signal when the temperature indicated by the temperature sensor is above a second temperature limit value.

In another embodiment, the invention provides a method that includes, measuring a temperature of an integrated circuit with a temperature sensor, the temperature sensor being part of the integrated circuit; comparing the measured temperature to a first temperature limit value stored in the integrated circuit; and generating a signal on a first output terminal of the integrated circuit according to the comparison. In one embodiment, the signal is asserted when the measured temperature is greater than the first temperature limit value. In one embodiment, the first signal on the output terminal is deasserted when a control location on the integrated circuit is accessed or when the measured temperature goes below a lower limit value, according to a programmable mode of operation.

The method may further include comparing the measured temperature to a second temperature limit value stored in the integrated circuit; and asserting a second signal on a second output terminal of the integrated circuit when the measured

temperature is above the second temperature limit value, thereby indicating that temperature has exceeded a safe limit.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings where the use of the same reference symbols in different drawings indicates similar or identical items.

FIG. 1 illustrates a high level block diagram of an exemplary system incorporating an embodiment of the present invention.

FIG. 2 illustrates an exemplary address block utilized in an embodiment of the present invention, to provide status, control, and temperature limit values.

FIG. 3 illustrates an exemplary control byte showing the control functions used in an embodiment of the invention.

FIG. 4 illustrates an exemplary system incorporating an embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

Referring to Fig. 1, a high level block diagram of an exemplary computer system is illustrated that incorporates an embodiment of the present invention. Integrated circuit 101, which in one preferred embodiment is a microprocessor, includes temperature sensor 103, which provides on-die thermal monitoring to measure the temperature of the die directly. There are a variety of approaches known in the art that can be used to implement a temperature sensor to directly measure the die temperature. For example, it is well known to use the voltage across a diode junction as an indication of temperature. In order to avoid temperature calibration for such a sensor, one approach supplies two different voltages to the diode and the difference in the two voltages measured indicates the temperature of the diode junction.

The temperature measurement, regardless of the type of temperature sensor, is compared to temperature limit values from registers 105 in compare logic 107. The compare logic determines if the measured temperature is above or below thresholds established in limit registers 105. Based on that comparison, processor output terminals 112 and 114 are driven to indicate the needed system action to be taken such as activating or deactivating a cooling device 109.

One of the limit values may be a panic limit value indicating a threshold temperature for safe processor operation. If the panic limit value is exceeded by the measured temperature, TPANIC output terminal 112 is asserted. Another of the output terminals, TALERT output terminal 114, may be used in several modes as explained further herein to provide thermal control information.

In an embodiment, various limit values and control functions can be programmably controlled in the microprocessor. Referring to Fig. 2, an exemplary address block 200 is illustrated that provides registers used for the various functions associated with the thermal control functions described herein. Note that while address block 200 may be implemented as a plurality of contiguous bytes, each of the described fields may be independently addressable. In one implementation each of the illustrated fields is byte length.

Referring to Figs. 1 and 2, temperature sensor 103 provides the current temperature measurement which, in one implementation, is expressed as an unsigned 7-bit value to temperature field 202 in address block 200. That register may be read by the processor to determine the current temperature indicated by temperature sensor 103.

Register 203 stores a programmable panic limit, which indicates a safe limit of operation. In one embodiment, the panic limit is implemented as a seven bit unsigned number and is preferably implemented as a read/write field. Operating the processor above the panic limit risks thermal damage to the processor. Thus, output terminal TPANIC 112 is asserted when compare logic 107 indicates the current temperature has exceeded the safe limit of safe operation. Assertion of TPANIC output terminal 112 should activate hardware and/or software to take immediate and possibly drastic actions to avoid thermal damage to the processor. For example, TPANIC may be

used to drive an interrupt or may be connected directly to a cooling device. TPANIC may also be used to shut down the power supply to avoid potential damage, if necessary. Once asserted, TPANIC can be cleared by writing (or otherwise accessing) a control bit in the processor.

Registers 205 and 207 store, respectively a lower limit temperature value and an upper limit temperature value. In one embodiment, each limit value is implemented as a seven bit unsigned number. The measured temperature value from temperature sensor 103 is compared to the upper and lower limit values that are written to registers 205 and 207. The comparison result is used to drive the output terminal TALERT 114. As previously mentioned, TALERT output terminal 114 can operate in several modes, a "thermostat" mode and an "interrupt" mode.

In thermostat mode, TALERT is asserted when the die temperature as measured by temperature sensor 103, rises above the upper limit value in register 207 and is deasserted when die temperature falls below the lower limit value defined in lower limit register 205. In thermostat mode, TALERT can be used to control a cooling fan or other cooling device, much like the thermostat in a building turns the air conditioning on and off to maintain the room temperature within an appropriate range.

In interrupt mode, TALERT is asserted when the die temperature rises above the upper limit value specified in upper limit register 207 and is de-asserted when software writes a control bit described further herein. In interrupt mode, TALERT may be used as a hardware interrupt signal. In response to assertion of TALERT, an interrupt service routine activates a cooling device as needed. The same service routine would be responsible for accessing a location, e.g., writing a register bit, that deasserts TALERT and its hardware interrupt.

A status field is supplied in 201 that supplies the status of both TALERT and TSTATUS (one bit each), i.e., whether the respective output terminal is asserted. Note that the panic limit and lower and upper limit registers are shown generically as temperature limit registers 105 in Fig. 1.

Address block 200 also includes control register 209, which has 8 control bits used in compare logic 107 to control the function of TALERT and TPANIC output terminals. The control bits are illustrated in more detail in Fig. 3. While not specifically illustrated, compare logic 107 or logic associated therewith is assumed to have the necessary control logic to provide the control functions defined in control byte 209. The individual bits of control register 209 will now be described.

Five bits of control register 209 are used to control TALERT output terminal 114. Referring to Fig. 3, the set alert when temperature is greater than the upper limit (SAGL) bit 303, when set, causes TALERT to be asserted when the measured temperature exceeds the upper limit value written into the upper limit register 207. The clear TALERT when temperature is less than lower limit (CALH) bit, 305, when set, causes the TALERT terminal to clear when the measured temperature falls below the lower limit value in lower limit register 205. The setting of CALH bit 305, in conjunction with the setting of the SAGL bit 303, causes TALERT to operate in thermostat mode. If CALH bit 305 is not set and SAGL bit 303 is set, TALERT operates in interrupt mode. The reset alert (RA) bit 301 is the control bit that is written when TALERT is used in interrupt mode to deassert TALERT. The alert polarity bit (AP) 302 specifies whether the TALERT output terminal is active high or low.

In one embodiment, control logic can be programmed so TALERT is asserted when the measured temperature falls below a programmed value rather than rises above a programmed value. Thus, in an example of such an embodiment, the set alert when temperature is less than the lower limit (SALH) bit 304, when set, causes TALERT to be asserted when the measured temperature is less than the lower limit in lower limit register 205. In such an embodiment, TALERT could be used to inhibit a fan (or other cooling device) when asserted, since the processor temperature is at a safe level. Using TALERT to inhibit cooling provides assurance that the cooling device is operating during boot-up prior to programming of the control register. In addition, if a "hang" occurs on boot-up and the registers are never programmed, the cooling device(s) are operating and the system is not at risk.

Three control bits in the illustrated embodiment are used to control operation of TPANIC output terminal 112. The set TPANIC when temperature is greater than the panic limit (SPGL) bit 308 enables operation of the TPANIC output terminal. As previously mentioned, once TPANIC output terminal 112 is asserted, accessing (e.g., writing) a control location such as the Reset Panic (RP) 306 bit can be used to reset the TPANIC output terminal 112. The TPANIC polarity bit 307 determines the polarity of an asserted TPANIC signal.

In an embodiment of the invention, all of the features can be disabled by resetting or not setting the appropriate control bit. Thus, in such an embodiment, if not intentionally enabled, the TALERT and TPANIC capability remains inactive. Thus, a processor according to an embodiment of the invention, can function in old system boards without design modifications.

The registers, bytes and/or bits used to monitor and control the thermal capabilities described herein may be mapped into processor input/output space at an offset from an I/O location set in a model specific register (MSR). In that way, it should be possible for the basic input/output system (BIOS) to map the thermal register(s) in a manner that does not interfere with other I/O devices or require new hardware to be added to system designs. Likewise, the BIOS should be able to re-map other I/O devices so they do not interfere with the chosen addresses for the thermal registers. Thus, in one embodiment, the ability is given to access the thermal registers through mapped I/O space in a way that does not interfere with other system I/O devices or require new hardware to be added to system designs. Alternatively, the registers containing the thermal control and status information shown in Figs. 2 and 3 may reside in one or more model specific registers, whose access may be restricted to software having the appropriate privilege level.

Referring to Fig. 4, an exemplary mobile system incorporating an embodiment of the present invention is illustrated. Processor 401 supplies TALERT output signal 402, which is coupled to directly control the speed of fan 405 through AND gate 407. A PIIX4 compatible input/output integrated circuit 409, known in the art as a South Bridge, receives the TPANIC alert 403 and performs an appropriate thermal failsafe action, e.g., stopping processor operations, if necessary, to safeguard the system when

the TPANIC alert 403 is asserted. AND gate 407 also receives a general purpose output (GPOn) control from South Bridge 409, which can be used to enable direct control by processor 401 of fan 405. South Bridge 409 performs other power management functions in the system, known in the art, which are not necessary for understanding of the present invention and thus are not described herein. In operation, BIOS post code can set the I/O address(es) for the thermal logic and setup the appropriate thermal management mode. In one embodiment, Advanced Configuration and Power Interface (ACPI) software, which enables the operating system to control the power management functions within the system, can be used to monitor die temperature. In a passive cooling mode, ACPI can throttle processor operations, i.e., reduce effective clock frequency using the STPCLK# input in response to die temperature. In active cooling modes fan 405 can be controlled directly by TALERT 402 as illustrated.

Thus, an on-board temperature sensor system has been described that provides more accurate and simpler thermal control functions. The ability to locate the sensor and the thermal registers (including the limit and control registers) on the processor and making the thermal control registers readily accessible to software operating on the processor, such as software implementing ACPI, simplifies thermal management of the computer system and provides more flexible thermal management capabilities.

The description of the invention set forth herein is illustrative, and is not intended to limit the scope of the invention as set forth in the following claims. For instance, the temperature logic, while described with relation to a processor, may be implemented on other integrated circuits. Further, the control registers may be implemented in a variety of manners as would be known to one of skill in the art. Some or all of the temperature control functions described herein may be implemented in a particular design based on system requirements. Note also that numerous variations of on-chip thermal sensors are known in the art. All such variations are included within the spirit and scope of the present invention. Other variations and modifications of the embodiments disclosed herein, may be made based on the description set forth herein, without departing from the scope and spirit of the invention as set forth in the following claims.

WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a temperature sensor providing a temperature measurement of the integrated circuit;

a programmable storage location storing a first temperature limit value, the programmable storage location accessible via an instruction executed by the integrated circuit; and

compare logic coupled to the temperature sensor and the storage location to provide an indication of a comparison between the temperature measurement and the first temperature limit value.

2. The integrated circuit as recited in claim 1 wherein the integrated circuit asserts a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement is above the first temperature limit value.

3. The integrated circuit as recited in claim 2 wherein the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, when the temperature measurement indicated by the temperature sensor falls below a programmable second temperature limit value.

4. The integrated circuit as recited in claim 2 wherein the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, in response to access to a control location in the integrated circuit.

5. The integrated circuit as recited in claim 2 wherein the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, when the temperature measurement falls below a programmable second temperature limit value or when a control location in the integrated circuit is accessed, according to a programmable mode of operation.

6. The integrated circuit as recited in claim 2 wherein the first temperature limit value is a panic value indicating a temperature limit for safe integrated circuit operation.

7. The integrated circuit as recited in claim 1 further comprising an addressable storage location coupled to the temperature sensor, the addressable storage location accessible by an instruction executed the integrated circuit and supplying an indication of the temperature measurement on the integrated circuit.

8. The integrated circuit as recited in claim 1 further comprising:
a second output terminal coupled to provide external to the integrated circuit an asserted signal when the temperature measurement indicated by the temperature sensor is above a second temperature limit value.

9. The integrated circuit as recited in claim 8 further comprising:
a second storage location supplying the second temperature limit value; and
second compare logic coupled to the second storage location and coupled to receive the temperature measurement of the integrated circuit, and wherein the second compare logic generates a second indication of when the temperature measurement of the integrated circuit is above the second temperature limit value.

10. The integrated circuit as recited in claim 9 further comprising:
a third storage location supplying a third temperature limit value;
third compare logic coupled to the third storage location and coupled to receive the temperature measurement, and wherein the compare logic generates a third indication that the temperature measurement of the integrated circuit is below the third temperature limit value.

11. The integrated circuit as recited in claim 1 wherein the integrated circuit asserts a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement indicated by the temperature sensor is below the third temperature limit value.

12. The integrated circuit as recited in claim 1 wherein the integrated circuit is a microprocessor.

13. A method comprising:
measuring a temperature of an integrated circuit with a temperature sensor, the temperature sensor being a circuit within the integrated circuit;
comparing the measured temperature to a first limit value stored in the integrated circuit; and
generating a signal on a first output terminal of the integrated circuit according to the comparison to control the temperature of the integrated circuit.

14. The method as recited in claim 13 wherein the signal is asserted when the measured temperature is less than the first limit value.

15. The method as recited in claim 14 wherein the asserted signal is used to inhibit a cooling device to control the temperature of the integrated circuit.

16. The method as recited in claim 13 wherein the signal is asserted when the measured temperature is greater than the first limit value.

17. The method as recited in claim 16 wherein the signal on the first output terminal is deasserted when a control location on the integrated circuit is accessed or when the measured temperature goes below a lower limit value, according to a programmable mode of operation.

18. The method as recited in claim 16 wherein the signal is utilized to directly control a cooling device.

19. The method as recited in claim 16 further comprising:
comparing the measured temperature to a lower limit value; and
deasserting the signal when the measured temperature is below the lower limit value.

20. The method as recited in claim 16 further comprising accessing a control location in the integrated circuit to cause the signal to be deasserted.

21. The method as recited in claim 16 wherein the asserted signal causes assertion of an interrupt and wherein a sequence of instructions, responsive to the asserted interrupt, activates a cooling device.

22. The method as recited in claim 21 wherein an instruction sequence causes the signal to be deasserted.

23. The method as recited in claim 13 further comprising:
comparing the measured temperature to a second limit value stored in the integrated circuit; and
asserting a second signal on a second output terminal of the integrated circuit when the measured temperature is above the second limit value, thereby indicating that temperature has exceeded a safe limit.

24. The method as recited in claim 23 wherein the second signal is deasserted by accessing a control location in the integrated circuit.

25. An apparatus comprising:
a processor including,
means for measuring temperature of the processor and providing a measured temperature;
means for comparing the measured temperature to at least two limit values; and
two output terminals on the processor coupled to supply an indication of results the comparison.

26. The apparatus as recited in claim 25 wherein the apparatus is a computer system and further comprises at least one cooling device, which activates in response to an asserted signal on at least one of the two output terminals.

27. A microprocessor comprising:

a temperature sensor providing a temperature measurement of the integrated circuit;

at least a first and second temperature limit value stored in programmable storage locations in the microprocessor, the storage locations being accessible via software executed by the microprocessor;

compare logic coupled to the temperature sensor and to the programmable storage locations storing the first and second temperature limit values, to provide respectively a first and second signal indicative of a comparison between the temperature measurement and the first and second temperature limit values; and

first and second output terminals coupled to provide respectively, the first and second signals.

28. The microprocessor as recited in claim 27 wherein the microprocessor deasserts the first signal, which is supplied on the first output terminal of processor, when the temperature measurement falls below a programmable third temperature limit value, thereby providing a thermostat mode of operation for the first signal.

29. The integrated circuit as recited in claim 27 wherein the microprocessor includes a software accessible control register controlling operation of the compare logic and the first and second output terminals.

METHOD AND APPARATUS FOR USING AN ON-BOARD TEMPERATURE SENSOR ON AN INTEGRATED CIRCUIT

Charles W. Mitchell
Patrick Maupin
Dervinn Caldwell

ABSTRACT OF THE DISCLOSURE

An integrated circuit such as a processor measures its own temperature with a temperature sensor. The measured temperature is compared to an upper limit value stored in the integrated circuit. An output terminal of the integrated circuit is asserted according to the comparison. In one mode of operation, the output terminal is asserted when the measured temperature is greater than the upper limit value and deasserted when the measured temperature goes below a lower limit value. A second output terminal is asserted when the temperature is above a second upper limit value, thereby indicating that temperature has exceeded a safe limit.

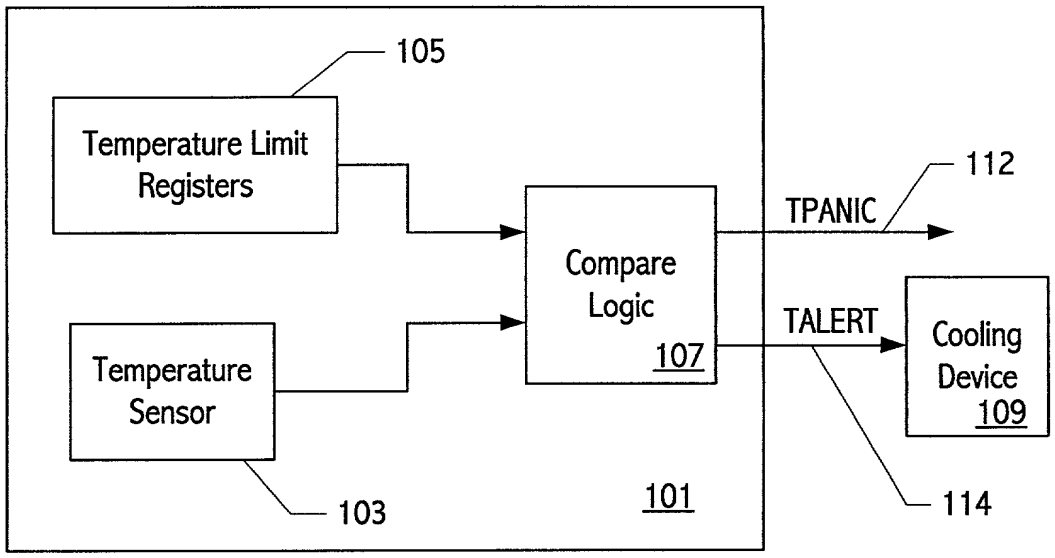
105
Temperature Limit Registers
112
TPANIC
Compare Logic
107
TALERT
Cooling Device
109
Temperature Sensor
103
101
114

FIG. 1

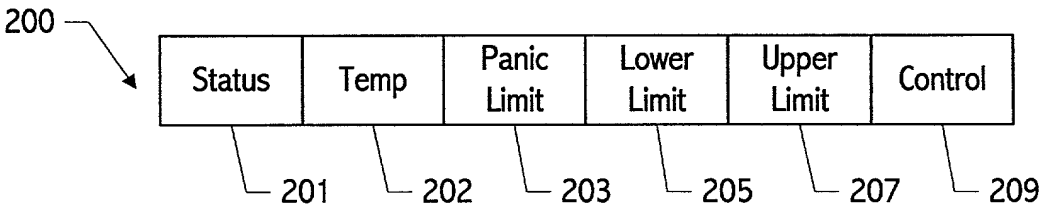
200
Status
Temp
Panic Limit
Lower Limit
Upper Limit
Control
201
202
203
205
207
209

FIG. 2

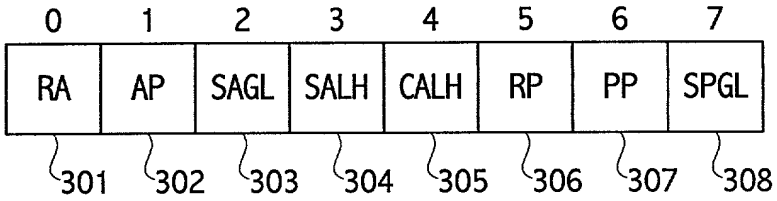
0
1
2
3
4
5
6
7
RA
AP
SAGL
SALH
CALH
RP
PP
SPGL
301
302
303
304
305
306
307
308

FIG. 3

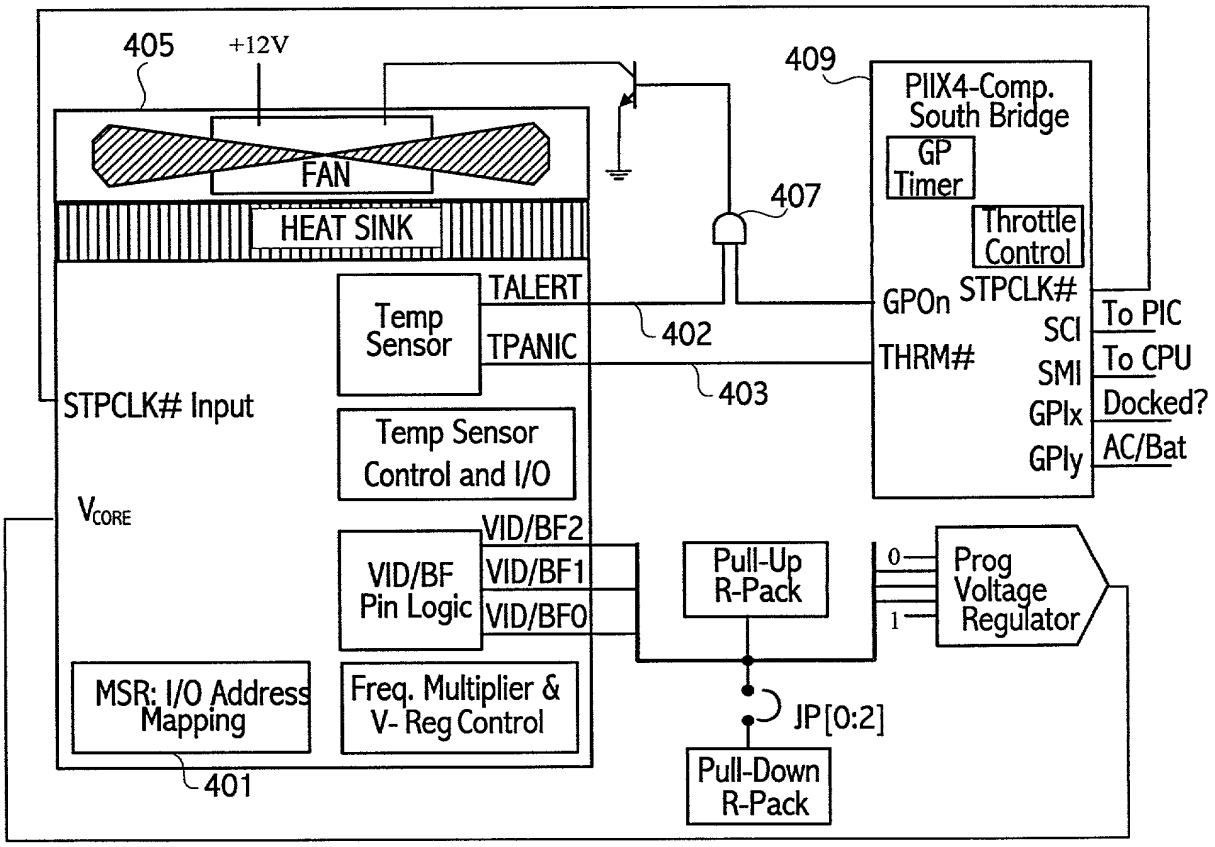
405
+12V
FAN
HEAT SINK
409
PIIX4-Comp.
South Bridge
GP
Timer
Throttle
Control
407
Temp
Sensor
TALERT
TPANIC
402
403
GPOn
STPCLK#
THRM#
SCI
SMI
GPIx
GPIy
To PIC
To CPU
Docked?
AC/Bat
STPCLK# Input
Temp Sensor
Control and I/O
VCORE
VID/BF2
VID/BF
Pin Logic
VID/BF1
VID/BF0
Pull-Up
R-Pack
0
1
Prog
Voltage
Regulator
MSR: I/O Address
Mapping
Freq. Multiplier &
V- Reg Control
JP[0:2]
Pull-Down
R-Pack
401

FIG. 4

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled

METHOD AND APPARATUS FOR USING AN ON-BOARD TEMPERATURE SENSOR ON AN INTEGRATED CIRCUIT

which (check) ☒ is attached hereto.
☐ and is amended by the Preliminary Amendment attached hereto.
☐ was filed on _____ as Application Serial No. _____
☐ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A				

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

Mark Zagorin (36,067); Andrew C. Graham (36,531); David W. O'Brien (40,107); Paul S. Drake (33,491); Louis A. Riley (39,817); William D. Zahrt, II (26,070); Richard J. Roddy (27,688); Harry A. Wolin (32,638); and Elizabeth A. Apperley (36,428).

Please direct all correspondence concerning this application to the USPTO Customer Number, if provided, or otherwise to the individual and/or firm named below:

Customer Number 22120
ZAGORIN, O'BRIEN & GRAHAM, L.L.P.
401 WEST 15TH STREET, SUITE 870
AUSTIN, TX 78701

Telephone: (512) 347-9030
Facsimile: (512) 347-9031

USPTO Customer Number
22120
PATENT TRADEMARK OFFICE

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole (or first joint) inventor: Charles W. Mitchell

Inventor's Signature: Charles W. Mitchell Date: Sept. 8, 2000
Residence: Austin, Texas Citizenship: USA
Post Office Address: 6501 Skinner Cove
Austin, TX 78759

Full name of second joint inventor: Patrick Maupin

Inventor's Signature: _____ Date: _____
Residence: Austin, Texas Citizenship: USA
Post Office Address: 5216 Crooked Oak Cove
Austin, TX 78749

Full name of third joint inventor: Dervinn Caldwell

Inventor's Signature: _____ Date: _____
Residence: Freemont, CA Citizenship: USA
Post Office Address: 3837 Burton Common
Fremont, CA 94536

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled

METHOD AND APPARATUS FOR USING AN ON-BOARD TEMPERATURE SENSOR ON AN INTEGRATED CIRCUIT

which (check) ☒ is attached hereto.
☐ and is amended by the Preliminary Amendment attached hereto.
☐ was filed on _____ as Application Serial No. _____
☐ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A				

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

Mark Zagorin (36,067); Andrew C. Graham (36,531); David W. O'Brien (40,107); Paul S. Drake (33,491); Louis A. Riley (39,817); William D. Zahrt, II (26,070); Richard J. Roddy (27,688); Harry A. Wolin (32,638); and Elizabeth A. Apperley (36,428).

Please direct all correspondence concerning this application to the USPTO Customer Number, if provided, or otherwise to the individual and/or firm named below:

Customer Number 22120
ZAGORIN, O'BRIEN & GRAHAM, L.L.P.
401 WEST 15TH STREET, SUITE 870
AUSTIN, TX 78701

Telephone: (512) 347-9030
Facsimile: (512) 347-9031

USPTO Customer Number
22120
PATENT TRADEMARK OFFICE

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole (or first joint) inventor: Charles W. Mitchell

Inventor's Signature: _____ Date: _____
Residence: Austin, Texas Citizenship: USA
Post Office Address: 6501 Skinner Cove
Austin, TX 78759

Full name of second joint inventor: Patrick Maupin

Inventor's Signature: Patrick Maupin Date: 9/12/2000
Residence: Austin, Texas Citizenship: USA
Post Office Address: 5216 Crooked Oak Cove
Austin, TX 78749

Full name of third joint inventor: Dervinn Caldwell

Inventor's Signature: _____ Date: _____
Residence: Freemont, CA Citizenship: USA
Post Office Address: 3837 Burton Common
Fremont, CA 94536

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled

METHOD AND APPARATUS FOR USING AN ON-BOARD TEMPERATURE SENSOR ON AN INTEGRATED CIRCUIT

which (check) ☒ is attached hereto.
☐ and is amended by the Preliminary Amendment attached hereto.
☐ was filed on _____ as Application Serial No. _____
☐ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A				

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

Mark Zagorin (36,067); Andrew C. Graham (36,531); David W. O'Brien (40,107); Paul S. Drake (33,491); Louis A. Riley (39,817); William D. Zahrt, II (26,070); Richard J. Roddy (27,688); Harry A. Wolin (32,638); and Elizabeth A. Apperley (36,428).

Please direct all correspondence concerning this application to the USPTO Customer Number, if provided, or otherwise to the individual and/or firm named below:

Customer Number 22120
ZAGORIN, O'BRIEN & GRAHAM, L.L.P.
401 WEST 15TH STREET, SUITE 870
AUSTIN, TX 78701

Telephone: (512) 347-9030
Facsimile: (512) 347-9031

USPTO Customer Number
22120
PATENT TRADEMARK OFFICE

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole (or first joint) inventor: Charles W. Mitchell

Inventor's Signature: _____ Date: _____
Residence: Austin, Texas Citizenship: USA
Post Office Address: 6501 Skinner Cove
Austin, TX 78759

Full name of second joint inventor: Patrick Maupin

Inventor's Signature: _____ Date: _____
Residence: Austin, Texas Citizenship: USA
Post Office Address: 5216 Crooked Oak Cove
Austin, TX 78749

Full name of third joint inventor: Dervinn Caldwell

Inventor's Signature: Dervinn Caldwell Date: 8/31/00
Residence: Freemont, CA Citizenship: USA
Post Office Address: 3837 Burton Common
Fremont, CA 94536